AMENDMENTS TO THE CLAIMS

1. (Currently amended) A liquid crystal panel for liquid crystal display devices comprising:

a lower substrate including a seal pattern forming region between a display area and a non-display area of the lower substrate, wherein a passivation layer is removed in the non-display region;

an upper substrate;

a seal pattern formed in a boundary region between the display area and the non-display area of the lower substrate; and

a liquid crystal layer between the upper substrate and the lower substrate.

2. (Original) The device according to claim 1, wherein the lower substrate further includes a first substrate, the display area and the non-display area.

3. (Original) The device according to claim 2, wherein the lower substrate further includes a gate electrode on the first substrate, a gate insulating layer on the first substrate and on the gate electrode, a thin film transistor on the gate insulating layer, a pixel electrode that is connected to the thin film transistor on the gate insulating layer and a passivation layer on the thin film transistor.

4. (Original) The device according to claim 1, wherein the upper substrate includes a second substrate, a color filter and a common electrode.

5. (Original) The device according to claim 1, wherein the passivation layer in the boundary region between the display area and the non-display area of the lower substrate is removed during a photolithographic mask step for simultaneous patterning an active layer and the passivation layer.

6. (Original) The device according to claim 1, wherein the liquid crystal panel of the present invention further comprises spacers between the upper substrate and the lower substrate.

7. (Currently amended) A fabricating method for a liquid crystal panel for liquid crystal display devices comprising:

forming a lower substrate wherein a passivation layer in a boundary region between a display area and a non-display area of the lower substrate is removed;

forming an upper substrate including a second substrate, a color filter and a common electrode;

forming spacers in the display area between the upper substrate and the lower substrate;

forming a seal pattern in [[a]] the boundary region between the display area and the non-display area of the lower substrate, the seal pattern contacting a gate insulating layer;

assembling the upper substrate and the lower substrate; and

injecting liquid crystal into an interior of the seal pattern.

8. (Original) The method according to claim 7, wherein the forming the lower substrate further comprises:

forming a gate electrode on a first substrate;

forming a gate insulating layer on the first substrate and on the gate electrode;

forming a thin film transistor on the gate insulating layer; and

forming a pixel electrode on the gate insulating layer, the pixel electrode being connected to the thin film transistor.

9. (Currently amended) A liquid crystal panel for liquid crystal display devices comprising:

a lower substrate including a first substrate;

a gate electrode on the first substrate;

a gate insulating layer on the first substrate and on the gate electrode;

a thin film transistor on the gate insulating layer;

a pixel electrode on the gate insulating layer, the pixel electrode being connected to the thin film transistor;

a passivation layer on the thin film transistor, the lower substrate being divided into a display area and a non-display area and further including a seal pattern forming region between the display area and the non-display area of the lower substrate, wherein a passivation layer is removed in the seal pattern forming region;

an upper substrate including a second substrate, a color filter and a common electrode;

a seal pattern formed in a boundary region between the display area and the non-display area of the lower substrate; and

a liquid crystal layer between the upper substrate and the lower substrate.

10. (previously presented) A liquid crystal panel comprising:

a lower substrate having a display area and a non-display area;

an upper substrate having an area corresponding to the display area, the upper substrate and the lower substrate spaced apart and facing each other;

a seal pattern formed between the upper substrate and the lower substrate along a boundary region between the display area and the non-display area, the seal pattern having an injection hole; and

liquid crystal injected to a liquid crystal cell through the injection hole, wherein a seal is formed to seal the injection hole, the seal pattern serving to make a cell gap for injecting the liquid crystal and to bond the upper substrate and the lower substrate,

wherein a passivation layer is removed in the boundary region.

11. (Original) The liquid crystal panel of claim 10, wherein the seal pattern is formed by a screen printing process using thermosetting resin that includes glass fiber.

12. (Currently amended) A liquid crystal panel comprising:

an upper substrate and a lower substrate spaced apart and facing each other;

a gate electrode formed on a transparent substrate of the lower substrate, and a gate insulating layer formed on an entire area of the lower substrate and on the gate electrode; a thin film transistor including the gate electrode formed on the gate insulating layer;

a pixel electrode connected to the thin film transistor;

a seal pattern formed between the upper substrate and the lower substrate and in contact with the gate insulating layer along a boundary between a display area and a non-display area; and

a spacer disposed in the display area to uniformly maintain a cell gap distance between the upper substrate and the lower substrate,

13. (Currently amended) A liquid crystal panel comprising:

a horizontal gate line that includes a gate electrode and a capacitance electrode formed on an array substrate;

a vertical data line that includes a drain electrode and formed on the array substrate, the data line crossing the gate line;

a data pad formed at one end of the data line;

a source electrode spaced apart from the drain electrode, and a pixel electrode connected to the source electrode and partially overlapped with the capacitance electrode;

a semi-conductor layer formed under the source and drain electrodes and the thin film transistor including the gate electrode;

an auxiliary capacitance electrode connected to the pixel electrode and formed between the capacitance electrode and the pixel electrode;

a seal pattern formed between the data pad and an adjacent portion of the data line to assemble the upper substrate and the lower substrate with a uniform cell gap, the seal pattern dividing the array substrate into a display area and a non-display area;

a passivation layer removed ~~where electric lines are not formed, the removal of the passivation layer maintaining cell gap distances between the display area and~~ in the seal pattern forming region.

14. (Original) A liquid crystal panel comprising:

an upper substrate and a lower substrate spaced apart and facing each other;

a spacer disposed between the upper substrate and the lower substrate to uniformly maintain a cell gap;

a storage capacitor region including a capacitance electrode formed on a transparent substrate;

a gate insulating layer formed on the transparent substrate and on the capacitance electrode;

a semi-conductor layer formed on the gate insulating layer and an auxiliary capacitance electrode formed on the semi-conductor layer;

a passivation layer formed on the auxiliary capacitance electrode and a pixel electrode formed on the passivation layer, the pixel electrode contacting a lateral side of the auxiliary capacitance electrode.

15. (Original) The liquid crystal panel according to claim 14, further comprising a thin film transistor region including:

a gate electrode formed on the transparent substrate, and the gate insulating layer formed on the transparent substrate and on the gate electrode;

a source electrode and a drain electrode spaced apart from each other and formed on the semi-conductor layer.

16. (Original) The liquid crystal panel according to claim 14, wherein the semi-conductor layer includes an active layer and an ohmic contact layer, the semi-conductor layer being formed on the gate insulating layer.

17. (Original) The liquid crystal panel according to claim 14, wherein only the gate insulating layer is formed on the transparent substrate in the boundary region between the display area and the non-display area to maintain the cell gap distance uniformly.

18. (Currently amended) A fabricating process of a liquid crystal panel for liquid crystal display devices comprising:

a first step including:

preparing upper and lower substrates, the lower substrate including a first substrate divided into a display area and a non-display area, a gate insulating layer formed on the first substrate and a thin film transistor formed on the gate insulating layer, a pixel electrode connected to the thin film transistor and formed on the gate insulating layer, a passivation layer formed on the thin film transistor, the passivation layer removed from[[on]] a seal pattern forming region ~~and being exposed to light to be etched away~~ during a photolithographic masking process, the seal pattern formed directly on the gate insulating layer, the upper substrate having an area corresponding to the display area of the lower substrate, the upper substrate including a second substrate, a color filter and a common electrode;

a second step including:

providing spacers dispensed on the display area; and

forming a seal pattern having an injection hole,

wherein the spacer dispensing and the seal pattern forming processes are performed on one of only one substrate or on both the upper substrate and the lower substrate, respectively;

a third step including:

injecting a liquid crystal into an interior of the seal pattern; and

sealing the injection hole of the seal pattern.

19. (previously presented) The fabricating process of a liquid crystal panel according to claim 18, wherein an alignment layer coating process and a rubbing process precedes the spacer dispensing process and the seal pattern forming process.

20. (previously presented) The fabricating process of a liquid crystal panel according to claim 18, wherein the passivation layer and the active layer are patterned simultaneously according to a four mask process and only the gate insulating layer exists under the pixel electrode that is connected to the storage capacitor and the thin film transistor.